Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1. (Currently amended) A method in a data processing system for processing instructions, the method comprising:

responsive to receiving an initial instruction for execution in an instruction cache in a processor in the data processing system, determining whether the initial instruction indicates enabling a mode of operation in which interrupts are to be generated;

if the initial instruction indicates enabling a mode of operation in which interrupts are to be generated, ~~responsive to~~ receiving a subsequent instruction; ~~after receiving the instruction,~~

determining whether the subsequent instruction is of a ~~certain~~ type selected for analysis; and

generating an interrupt if the ~~mode of operation in which interrupts are to be enabled and the~~ subsequent instruction is determined to be of ~~the certain~~ a type selected for analysis.

2. (Currently amended) The method of claim 1 further comprising:

~~responsive to receiving a subsequent instruction in the subsequent instructions indicating disablement of the mode of operation in which interrupts are to be generated,~~ disabling the mode of operation in which interrupts are to be generated if the subsequent instruction is determined to be of a type to disable the mode of operation in which interrupts are to be generated.

3. (Original) The method of claim 1, wherein the generating step comprises:

sending a signal from an instruction cache to an interrupt unit in the processor; and

processing the interrupt in the interrupt unit in response to receiving the signal at the interrupt unit.

4. (Original) The method of claim 3, wherein the processing step includes:

executing code associated with the interrupt.

5. (Original) The method of claim 4, wherein the code records cache misses by a functional unit attempting to access instructions in a cache.

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6. (Currently amended) The method of claim 4, wherein the code counts a number of times the subsequent instruction of the ~~certain~~ type selected for analysis has been executed.

7. (Canceled)

8. (Currently amended) The method of claim 1, wherein the subsequent instruction of the ~~certain~~ type selected for analysis is a branch instruction.

9. (Canceled)

10. (Currently amended) A data processing system for processing instructions, the data processing system comprising:

first determining means, responsive to receiving an initial instruction for execution in an instruction cache in a processor in the data processing system, for determining whether the initial instruction indicates enabling a mode of operation in which interrupts are to be generated;

~~second determining~~ receiving means~~, responsive to~~ for receiving a subsequent instruction if the initial instruction indicates enabling a mode of operation in which interrupts are to be generated ~~after receiving the instruction,~~;

second determining means for determining whether the subsequent instruction is determined to be of a ~~certain~~ type selected for analysis; and

generating means for generating an interrupt if the ~~mode of operation in which interrupts are to be enabled and the~~ subsequent instruction is determined to be of ~~the certain~~ a type selected for analysis.

11. (Currently amended) The data processing system of claim 10 further comprising:

disabling means~~, responsive to receiving a subsequent instruction in the subsequent instructions indicating disablement of the mode of operation in which interrupts are to be generated,~~ for disabling the mode of operation in which interrupts are to be generated if the subsequent instruction is determined to be of a type to disable the mode of operation in which interrupts are to be generated.

12. (Original) The data processing system of claim 10, wherein the generating means comprises:

sending means for sending a signal from an instruction cache to an interrupt unit in the processor; and

processing means for processing the interrupt in the interrupt unit in response to receiving the signal at the interrupt unit.

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13. (Original) The data processing system of claim 12, wherein the processing means includes: executing means for executing code associated with the interrupt.

14. (Original) The data processing system of claim 13, wherein the code records cache misses by a functional unit attempting to access instructions in a cache.

15. (Currently amended) The data processing system of claim 13, wherein the code counts a number of times the subsequent instruction of the ~~certain~~ type selected for analysis has been executed.

16. (Canceled)

17. (Currently amended) The data processing system of claim 10, wherein the subsequent instruction of the ~~certain~~ type selected for analysis is a branch instruction.

18. (Currently amended) A computer program product in a computer readable medium for processing instructions, the computer program product comprising:

first instructions, responsive to receiving an initial instruction for execution in an instruction cache in a processor in the data processing system, for determining whether the initial instruction indicates enabling a mode of operation in which interrupts are to be generated;

if the initial instruction indicates enabling a mode of operation in which interrupts are to be generated, second instructions~~, responsive to~~ for receiving a subsequent instruction; ~~after receiving the instruction,~~

third instructions for determining whether the subsequent instruction is of a ~~certain~~ type selected for analysis; and

~~third~~ fourth instructions, for generating an interrupt if the ~~mode of operation in which interrupts are to be enabled and the~~ subsequent instruction is determined to be of the ~~certain~~ type selected for analysis.

19. (Currently amended) The computer program product of claim 18 further comprising:

~~fourth~~ fifth instructions~~, responsive to receiving a subsequent instruction in the subsequent instructions indicating disablement of the mode of operation in which interrupts are to be generated,~~ for disabling the mode of operation in which interrupts are to be generated if the subsequent instruction is determined to be of a type to disable the mode of operation in which interrupts are to be generated.

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20. (Currently amended) The computer program product of claim 18, wherein the ~~third~~ fourth instructions comprises:

first sub-instructions for sending a signal from an instruction cache to an interrupt unit in the processor; and

second sub-instructions for processing the interrupt in the interrupt unit in response to receiving the signal at the interrupt unit.

21. (Original) The computer program product of claim 20, wherein the second sub-instructions includes:

instructions for executing code associated with the interrupt.

22. (Original) The computer program product of claim 21, wherein the code records cache misses by a functional unit attempting to access instructions in a cache.

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